UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,378	10/09/2003	Francesco Pappalardo	851763.443	6097

38106 7590 03/10/2006

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
KIM, KENNETH S	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,378	PAPPALARDO ET AL.	
	Examiner	Art Unit	
	Kenneth S. KIM	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Mar08'04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-23 are presented for examination.

2. The abstract of the disclosure is objected to because the current abstract does not reflect the inventive feature of the claimed invention to distinguish over the prior art. Correction is required. See MPEP § 608.01(b).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauer et al, U.S. Patent No. 6,049,862, cited by the applicant.

Bauer et al teaches the invention as claimed in claim 1 including a reconfigurable control structure for CPUs, comprising:

(a) a first control unit (7) with a first basic instruction set associated therewith (col. 4, line 24),

(b) a second control unit (8) with a second instruction set associated therewith (col. 4, line 50), a programming element associated with said second control unit for rendering said second instruction set selectively modifiable (col. 2, lines 23 and 30),

(c) at least one circuit element (4) for supplying instruction codes to be executed

to said first control unit and to said second control unit, so that each instruction can be executed under the control of at least one between said first control unit and said second control unit according to whether each instruction is comprised within at least one between said first basic instruction set and said second selectively modifiable instruction set (col. 4, line 5), and

further teaches as in claims 2-12,

(d) sending said instruction codes to be executed in a undifferentiated way to said first control unit and said second control unit (col. 4, line 5), and a selection module (9) configured for recognizing whether' the instruction belongs to said first basic instruction set or to said second selectively modifiable instruction set (col. 5, line 23) – claim 2,

(e) an output module (10) comprising a first set of input lines connected to an output of said first control unit, a second set of input lines connected to an output of said second control u nit, and a set of output lines, wherein said output module is connected to said selector module (9) for transferring on said set of output lines the signal present on said first set of input lines or ori said second set of input lines (col. 5, line 30) – claim 3,

(f) said first control unit and second control unit are configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in said first basic instruction set (an embodiment of a decoder) – claims 4, 6, and 9,

(g) said first control unit is configured as a wired-logic control unit (col. 4, line 24) – claim 5,

(h) said second control unit is basically configured as a micro-programmed-logic control unit (col. 4, line 40; micro-program stored in the cells) – claims 7 and 8,

(i) said second control unit is programmable, programming of said second control unit being carried out by said first control unit by means of instructions (col. 2, line 35; by hardwired decoder instructions), by means of an operation of memory programming (col. 2, lines 37 and 5) – claims 10 -12,

The process claims13-16 with instruction set identifier bit (col. 4, line 9) and the second instruction set replicating the first instruction set (can be any instruction set) for debugging or backup purpose (can be used for any purpose) and the structure claims 17-23 are equivalently rejected based on the same reason.

5. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kucukcakar et al, U.S. Patent No. 6,138,229.

Kucukcakar et al teaches the invention as claimed in claim 1 including a reconfigurable control structure for CPUs, comprising:

(a) a first control unit (46) with a first basic instruction set associated therewith (col. 3, line 53),

(b) a second control unit (48) with a second instruction set associated therewith (col. 3, line 55), a programming element associated with said second control unit for rendering said second instruction set selectively modifiable (col. 2, line 1),

(c) at least one circuit element (col. 2, line 44) for supplying instruction codes to be executed to said first control unit and to said second control unit, so that each instruction can be executed under the control of at least one between said first control

unit and said second control unit according to whether each instruction is comprised within at least one between said first basic instruction set and said second selectively modifiable instruction set (col. 3, line 57), and

further teaches as in claims 2-12,

(d) sending said instruction codes to be executed in a undifferentiated way to said first control unit and said second control unit (col. 3, line 7), and a selection module (47) configured for recognizing whether the instruction belongs to said first basic instruction set or to said second selectively modifiable instruction set– claim 2,

(e) an output module (49) comprising a first set of input lines connected to an output of said first control unit, a second set of input lines connected to an output of said second control u nit, and a set of output lines, wherein said output module is connected to said selector module (9) for transferring on said set of output lines the signal present on said first set of input lines or ori said second set of input lines (col. 3, line 57) – claim 3,

(f) said first control unit and second control unit are configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in said first basic instruction set (an embodiment of a decoder) – claims 4, 6, and 9,

(g) said first control unit is configured as a wired-logic control unit (fixed) – claim 5,

(h) said second control unit is basically configured as a micro-programmed-logic control unit (can be implemented as a micro-program controlled decoder) – claims 7 and 8,

(i) said second control unit is programmable, programming of said second

control unit being carried out by said first control unit by means of instructions (col. 5, line 51; by
hardwired decoder instructions), by means of an operation of
memory programming (storing configuration data in FPGA memory) – claims 10 -12,

The process claims13-16 with instruction set identifier bit (bit in opcode) and the second instruction set replicating the first instruction set (can be any instruction set) for debugging or backup purpose (can be used for any purpose) and the structure claims 17-23 are equivalently rejected based on the same reason.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Studor et al taught a method of extending instruction set using second state sequencer.

Hammond et al taught a method of using two separate instruction set decoders.

Trimberger taught a method of using instruction set identifier bit (fig. 3) and programming under execution of a first instruction set (col. 4, line 4).

Shekels taught a method of using micro-tasked programmable decoder.

Murao et al taught a method of decoding two different groups of instructions.

Applicant is reminded that the submitted reference AP teaches finite state machine control units.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

***

March 1, 2006

KENNETH S. KIM
PRIMARY EXAMINER